## REMARKS

The application has been reviewed in light of the Office Action dated March 12, 2009. Claims 1-9 were pending. By this Amendment, claims 1 and 3 have been amended to place the claims in better form for examination, and claim 3 has been amended to include a feature of independent claim 1, and new claims 10 and 11 have been added. Claims 1-11 would be pending upon entry of this Amendment, with claims 1 and 3 being in independent form.

Claims 1, 3 and 7-9 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,218,222 to Roberts. Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by Usuki (JP 11-220094). Claims 3-6 and 8-9 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 4,757,363 to Bohm et al. Claim 7 was rejected under 35 U.S.C. § 102(b) as purportedly anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over, Bohm.

Roberts, as understood by applicant, proposes a circuit configured with ESD (electrostatic discharge) protection, as shown schematically in Fig. 1 of Roberts and a top view fabrication layout of which is provided in Fig. 2, wherein series resistor 12 is connected between input pad 11 and active output driver circuit 14 (comprising active pullup n-channel transistor 16 and active n-channel transistor 15 connected together by their drains at output node 17), and lateral n-p-n bipolar transistor 13 is connected between the output node of circuit 14 and $V_{SS}$ (the collector of the transistor 13 is connected to output node 17 as well as to resistor 12, the emitter of the transistor 13 is connected to $V_{SS}$ and the gate of the transistor 13 is connected to the silicon substrate of the device).

As shown in Figs. 3-6 of Roberts which show various composite cross-sectional views, the series resistor 12 is ***NOT*** formed on or in substrate 34. For example, the cross-sectional view

of Fig. 3 shows that insulating layer 33 is interposed between the substrate 34 and the series resistor 12.

Roberts simply does ***NOT*** disclose or suggest, *inter alia*, the aspect of the present application of a protection resistance formed on the substrate.

Likewise, Usuki (JP 11-220094) does not disclose or suggest, *inter alia*, the aspect of the present application of a protection resistance formed on the substrate.

Polysilicon layer 2 is equated in the Office Action with the protection resistance of the present application.

However, the polysilicon layer 2 is ***NOT*** formed on substrate 1 of Usuki, and instead is stratified above, but ***NOT*** on, the substrate 1, as shown in Fig. 3 of Usuki.

Applicant submits that the Roberts and Usuki, even when considered along with common sense and common knowledge to one skilled in the art, does ***NOT*** render unpatentable the above-mentioned aspect of each of independent claims 1 and 3 of the present application.

Bohm, as understood by applicant, proposes an input protection circuit, as illustrated in Fig. 1 of Bohm, wherein input is supplied from a bonding pad 12 through a resistor-diode protection circuit 14 to the input gates of a complementary insulated gate field effect transistor inverter 16, and an input series resistor RP of the resistor-diode protection circuit 14 is connected to a first voltage source $V_{CC}$ through a plurality of parallel resistor-diode combinations in which diodes D1 through DI+1 have an input series resistance RP1 through RPI+1 to the series input resistor RP and D1 through DI have an output series resistance RN1 through RNI, and the contact resistance to VCC is illustrated as resistor RN. Each of the distributive resistors RP1 through RPI+1 is formed by a P- region 22 and an N- substrate 20 and the series resistance is formed by a P+ region 24 formed in the P- region 22.

The series resistance formed by P+ region 24 in Bohm is equated in the Office Action with the protection resistance of the present application, and the inverter 16 in Bohm is equated in the Office Action with the internal circuitry region.

However, bonding pad 12 in the device of Bohm is NOT placed between the P+ region 24 and the inverter 16.

Bohm simply does ***NOT*** disclose or suggest, *inter alia*, the aspect of the present application that the pad is placed between the protection resistance and the internal circuitry region.

Applicant submits that Bohm, even when considered along with common sense and common knowledge to one skilled in the art, does ***NOT*** render unpatentable the above-mentioned aspect of each of independent claims 1 and 3 of the present application.

In view of the remarks hereinabove, applicant submits that the application is now allowable, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any required fees, and to credit any overpayment, to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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